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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,895	11/13/2003	Mitsuhiko Ogihara	MAE 300	6100

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EXAMINER	
PHAM, HAI CHI	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,895	OGIHARA ET AL.	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-31* is/are allowed.

6)☒ Claim(s) *1-5 and 8-27* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 06/12/06 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the copending application 10/701,622 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Objections

2. Claim 29 is objected to because of the following informalities:

- Line 5, "the circuit pattern" should read --a circuit pattern-- because of lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 8-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman et al. (U.S. 5,681,756) in view of Abe (U.S. 5,485,0210).

Norman et al. discloses an integrated multicolor or single color organic LED array comprising a substrate (12), a first semiconductor film (electron transport layer 14 and organic layer 15) (col. 3, lines 5-16) disposed on and bonded to the substrate, the first thin semiconductor film including at least one semiconductor device (each of the organic layers 15, 20, 25 corresponds to a particular color LED device), a second thin semiconductor film formed in the substrate, the second thin semiconductor film including an integrated circuit (integrated circuit driver using thin film transistor 50).

Norman et al. fails to teach the second thin semiconductor being formed on the surface of the substrate, the IC driver having a first terminal to be connected to the semiconductor device and the first individual interconnecting line formed as a thin film extending from the first semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first semiconductor film to the first terminal in the second thin semiconductor film, and the array of semiconductor devices pairing with the integrated circuits.

Abe discloses a semiconductor device comprising a substrate (31), a semiconductor device (LD) formed on the surface of the substrate and a thin semiconductor film (32) whose material is different from the semiconductor device and being bonded to the same surface of the substrate as the semiconductor device, the thin semiconductor film including an integrated circuit (33), wherein the semiconductor device is connected to interconnections of said integrated circuit (the terminal of the integrated circuit 33 is inherently included due to such connection) (see claim 1 starting

at col. 4, line 65). Abe further teaches the semiconductor devices being disposed in arrays pairing with the integrated circuits (Fig. 5).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Norman et al. by providing the second thin semiconductor film that includes the integrated circuit to be formed on and bonded to the surface of the substrate as taught by Abe. The motivation for doing so would have been to allow higher integration of the drive circuitry.

Norman et al. further teaches:

- a layer of conductive material (negative contact layer 13) disposed between the first semiconductor film (14) and the substrate (12), the layer of conductive material being bonded and formed on the substrate and the first semiconductor film being bonded to the layer of conductive material, whereby the first semiconductor film is bonded onto the substrate (Fig. 1),
- the layer of conductive material (13) is a metal layer (col. 2, lines 65-66),
- the substrate has glass, resin, a ceramic, metal, or a semiconductor as its principal material (substrate 12 including a semiconductor material such as silicon) (col. 2, lines 62-64),
- the first semiconductor film has amorphous silicon, monocrystalline silicon, polysilicon, a compound semiconductor, or an organic semiconductor as its principal material (the semiconductor device having an organic layer 15),
- the first thin semiconductor film is an epitaxially grown compound semiconductor film (organic layer),

- the semiconductor device in said first semiconductor film is one of a light-emitting device, a photodetector, a Hall element, and a piezoelectric device (the layer 15 being a luminescent hole transport layer and the layer 14 an electron transport layer providing the desired light emission) (col. 3, lines 25-28), and the integrated circuit (driver IC 50) in the second thin semiconductor film includes a driver circuit for driving the semiconductor device,
- the first semiconductor film includes a plurality of semiconductor devices disposed at regular intervals, said semiconductor device being one of the plurality of semiconductor devices (organic layers 15, 20 and 25 forming red, green and blue organic layers disposed at regular intervals where the positive electrodes 40, 35 and 30 are respectively located) (Fig. 6),
- the first semiconductor film includes only one said semiconductor device (e.g., layer 15),
- a plurality of first semiconductor films are bonded to said surface of the substrate, said first semiconductor film being one of the plurality of first thin semiconductor films (Fig. 6),
- the second thin semiconductor film (driver IC 50) having recrystallized silicon, monocrystalline silicon, polycrystalline silicon, a compound semiconductor, an organic semiconductor, or a polymer as its principal material (driver IC 50 consists essentially of FETs also known as metal oxide silicon FETs made of polycrystalline silicon),

- a plurality of first semiconductor films are bonded to said surface of the substrate, said first semiconductor film being one of the plurality of first semiconductor films, the plurality of first semiconductor films being disposed in a row array, the second semiconductor film having a length substantially equal to a length of the linear array (the LED array being arranged at least in one row and the corresponding driver IC 66 or 70 having the same length as the LED array) (Fig. 10).

Norman also teaches the first and second semiconductor films being less than or equal to ten micrometers thick (each of the layers 14 and 15 having a thickness of 200-700 angstroms or 0.02-0.07 micrometers) but fails to teach the upper limit of the thickness. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the proper thickness range for the semiconductor films as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claims 7 and 18, Norman et al. in view of Asada et al. discloses all the claimed structure of the semiconductor device, and "even though product-by-process claims are limited by and defined by the process, e.g., using photolithography for forming the individual interconnecting line, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product

was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (See MPEP 2113).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norman et al. in view of Abe, as applied to claim 1 above, and further in view of Sakai et al. (U.S. 6,633,322).

Norman et al., as modified by Abe, discloses all the basic limitations of the claimed invention except for the circuit pattern formed on the substrate and comprising at least one of an interconnecting line, a resistor, and a capacitor.

Sakai et al. discloses an optical head having a light emitting element array comprising a substrate (10), a first semiconductor film (light emitting element 3) disposed on and bonded to the substrate, the first semiconductor film including at least one semiconductor device (the light emitting device being a semiconductor device), a second semiconductor film formed in the substrate, the second thin semiconductor film including an integrated circuit (driving circuit 9 included an integrated circuit using thin film transistor circuit 4), and a first individual interconnecting line (wiring portions 6) formed as a thin film extending from an upside of the first semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first semiconductor film to the first terminal in the second thin semiconductor film, (wiring portions 6 made of metallic thin films connecting the light emitting element 3 to the driving circuit 9 from an upside of the device) (Fig. 1). Sakai et al. further teaches a circuit pattern (11) formed on the substrate (10) and

having an interconnecting line (12) electrically connecting the circuit pattern to the driving circuit (9).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the device of Norman et al. with the circuit pattern built on the substrate and the interconnecting line as taught by Sakai et al. for the purpose of allowing the semiconductor device to be interfaced with external driving device.

6. Claims 1, 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (U.S. 6,825,867) in view of Norman et al. and Abe.

Koga et al. discloses an image forming apparatus having an organic electroluminescent array exposure head (1), the apparatus includes at least a photosensitive drum (41), a developing device (44), and a transfer roller (66) (Fig. 7), wherein the exposure head comprises an array of organic EL light emitting elements (4) comprising a light emitting layer (10) and a hole injection layer (11) being bonded to the substrate (6) through the cathode layer (7), and a IC driver (5) made of thin film transistors.

However, Koga et al. fails to teach the IC driver having a first terminal to be connected to the semiconductor device and the first individual interconnecting line formed as a thin film extending from the first thin semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the

semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film.

Norman et al. discloses an integrated multicolor or single color organic LED array comprising a substrate (12), a first semiconductor film (electron transport layer 14 and organic layer 15) (col. 3, lines 5-16) disposed on and bonded to the substrate, the first thin semiconductor film including at least one semiconductor device (each of the organic layers 15, 20, 25 corresponds to a particular color LED device), a second thin semiconductor film formed in the substrate, the second thin semiconductor film including an integrated circuit (integrated circuit driver using thin film transistor 50).

On the other hand, Abe discloses a semiconductor device comprising a substrate (31), a semiconductor device (LD) formed on the surface of the substrate and a thin semiconductor film (32) whose material is different from the semiconductor device and being bonded to the same surface of the substrate as the semiconductor device, the thin semiconductor film including an integrated circuit (33), wherein the semiconductor device is connected to interconnections of said integrated circuit (the terminal of the integrated circuit 33 is inherently included due to such connection) (see claim 1 starting at col. 4, line 65). Abe further teaches the semiconductor devices being disposed in arrays pairing with the integrated circuits (Fig. 5).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Koga et al. with the aforementioned teachings of Norman et al. and Abe. The motivation for doing so would have been to form a compact semiconductor device while providing electrical

interconnection between the terminals of the semiconductors and that of the driver IC in an inexpensive and effective way without the need of forming bumps.

Allowable Subject Matter

7. Claims 28-31 are allowed.

8. Claims 6-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: claim 28 is patentable over the prior art of record because of the specific structure of the semiconductor device, which includes a semiconductor device formed by a first thin semiconductor film bonded on the surface of the substrate, an integrated circuit and a terminal provided with a second thin semiconductor device of a different material as the first thin semiconductor film, and a first individual interconnecting line formed as a thin film extending from an upside of the first thin semiconductor film over said surface of the substrate to an upside of the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film. The combined limitations as currently claimed are not taught by the prior art of record considered alone or in combination.

The primary reason for the indication of the allowability of claim 6 is the inclusion therein, in combination as currently claimed, of the limitation "a second individual interconnecting line formed as a thin film", which extends from the second thin

semiconductor film to the circuit pattern on the substrate, electrically interconnecting the second terminal with the third terminal, and which is not found taught by the prior art of record considered alone or in combination.

Claims 7 and 29-31 are allowable because they are dependent from claim 6 and 28 above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments with respect to claims 1-5 and 8-27 have been considered but are moot in view of the new grounds of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vip Patel can be reached on (571) 272-2458. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hai Pham

HAI PHAM
PRIMARY EXAMINER

August 18, 2006